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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/661,494	RHODES, HOWARD E.	
	Examiner	Art Unit	
	PAUL BERARDESCA	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *80-106* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *80-106* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Initially, the examiner would like to remind Applicant that because there was no traversal of the examiner's official notice statements in the previous office action in the arguments filed 3/11/2009, all features that were officially noted are now considered to be admitted prior art.

Applicant's arguments filed 3/11/2009 have been fully considered but they are not persuasive. Applicant argues that "the Hashimoto address circuit for the disclosed two-dimensional imaging array (to read pixels) is explained throughout the Hashimoto disclosure as requiring the vertical signal line, an odd row scanning line, an even row scanning line, and a row selection line…Hashimoto's address circuit is, therefore, different from that defined by the claim". The examiner cannot agree. Applicants have introduced the limitation "consisting of" to limit the first/second address circuits to exclusively include a first/second row select line and a shared column line. However, this does not distinguish the claim from Hashimoto. Because the combination of the odd-column scan line 58 and the vertical signal line 57 are used to address the first pixel, they read on claimed, **"first address circuit"**, wherein the first address circuit exclusively includes a first row select line (58) and a shared column line (57) as claimed. Likewise, because the even-column scan line 59 and the vertical signal line 57 are used to address the second pixel, they read on claimed, **"second address circuit"**,

wherein the second address circuit exclusively includes a second row select line (59) and a shared column line (57) as claimed.

In other words, it seems Applicant interprets an address circuit to be every element within the image sensor that is used to read out a pixel value, but the limitation "address circuit" is broad enough to cover any single circuit element or combination of circuit elements that is used in reading out a pixel. Therefore, although the row select line may need to be activated along with a scan line (58 or 59) and the vertical signal line 57 in order to read out a pixel, because the scan lines and vertical signal lines are used to read out the pixel, they can just as easily be interpreted as the **"address circuit"**, wherein Hashimoto discloses a row select line, a first address circuit, and a second address circuit.

Claim Objections

Claim 88 is objected to because of the following informalities: the limitations "said odd pixel" and "said even pixel" have no antecedent basis. Although the row is defined as having both odd and even pixels, an odd pixel and an even pixel are not defined in a singular form and therefore leaves ambiguity as to what the "said odd pixel" or "said even pixel" is. Therefore they assumed to be "an odd pixel" and "an even pixel" respectively. In addition, the limitation "the column lines of the first address circuit and the second address circuit" have no antecedent basis and are assumed to be "the shared column line of the first address circuit and the second address circuit". Appropriate correction is required. In addition, it is suggested that "a shared column

line" of the second address circuit be changed to "the shared column line" for clarity because it seems the first and second address circuits are using the same single column line.

Claim 97 is objected to because of the following informalities: the limitations "the first even row select line" and "the second odd row select line" have no antecedent basis and are assumed to be "the first even line" and "the second odd line" respectively. Appropriate correction is required.

Claim 102 is objected to because of the following informalities: the limitations "the first row select lines" and "the second row select lines" have no antecedent basis. Specifically, a first row select line and second row select line, both singular, have been defined prior, but plural row select lines have not been defined. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 80-96, 102-104, and 106 are rejected under 35 U.S.C. 102(e) as being anticipated by Hashimoto et al. (US Patent 6,977,684 B1) hereinafter referenced as Hashimoto.

Regarding claim 80, Hashimoto discloses an arrangement of circuits in pixels each circuit shared by plurality of pixels, in image sensing apparatus.

In addition, Hashimoto discloses, **"activating a first address circuit (58,57) for a first pixel of a pixel array (PD1,Mtx1,Mres,Msf,Msel) and a second address circuit (59,57) for a second pixel (PD2,Mtx2,Mres,Msf,Msel) adjacent said first pixel, said first pixel and said second pixel being in a row of pixels, said first address circuit consisting of a first row select line (58) and a shared column line (57), and said second address circuit consisting of a second row select line (59) and said shared column line (57) "**, as exhibited in figures 9-12.

In addition, Hashimoto discloses, **"activating at least one of first row select line (58) and the second row select line (59), wherein the first row select line (58) and the second row select line (59) each run along the row of pixels and are not connected to pixels of any other row of the array"**, as disclosed in column 11 lines 18-49 and exhibited in figures 2 and 9-12.

In addition, Hashimoto discloses, **"generating an output signal over the shared column line (57) corresponding to charge accumulated by at least one of the first pixel and the second pixel"**, as disclosed in column 11 lines 18-30 and exhibited in figures 9-12.

Regarding claim 81, Hashimoto discloses everything claimed as applied above (see claim 80), in addition, Hashimoto discloses wherein the shared column line (57) extends approximately linearly across the pixel array, which reads on claimed, **"wherein the shared column line extends approximately linearly across the pixel array",** as exhibited in figure 10.

Regarding 82, Hashimoto discloses everything claimed as applied above (see claim 81), in addition, Hashimoto discloses wherein the first and second row select lines (58,59) extend approximately linearly across the pixel array, which reads on claimed, **"wherein the first and second row select lines extend approximately linearly across the pixel array",** as exhibited in figure 10.

Regarding 83, Hashimoto discloses everything claimed as applied above (see claim 80), in addition, Hashimoto discloses wherein the first and second row select lines (58,59) extend approximately linearly across the pixel array, which reads on claimed, **"wherein the first and second row select lines extend approximately linearly across the pixel array",** as exhibited in figure 10.

Regarding claim 84, in addition, Hashimoto discloses focusing an image on an active pixel CMOS imager (optical system 21 focuses an image on CMOS sensor 22), the imager (22) comprising a pixel array, which reads on claimed, **"focusing an image**

on an active pixel CMOS imager, the imager comprising a pixel array", as exhibited in figures 1, 2, and 10.

Hashimoto discloses, **"activating a first address circuit (58,57) for a first pixel of a pixel array (PD1,Mtx1,Mres,Msf,Msel) and a second address circuit (59,57) for a second pixel (PD2,Mtx2,Mres,Msf,Msel) adjacent said first pixel, said first pixel and said second pixel being in a row of pixels, said first address circuit consisting of a first row select line (58) and a shared column line (57), and said second address circuit consisting of a second row select line (59) and said shared column line (57) "**, as exhibited in figures 9-12.

In addition, Hashimoto discloses activating a first pixel (PD1,Mtx1,Mres,Msf,Msel) in a row connected to a shared column line (57) using a first row select line (58) and then subsequently activating an adjacent second pixel (PD2,Mtx2,Mres,Msf,Msel) in the row connected to the shared column line (57) using a second row select line (59), the pixel array comprising the first and second pixels ([PD1,Mtx1,Mres,Msf,Msel], [PD2,Mtx2,Mres,Msf,Msel]) and the first row select line (58) and second row select line (59) each running along the length of the row and not being connected to pixels of any other row, which reads on claimed, **"addressing the first pixel using the first row select line and then subsequently addressing the second pixel using the second row select line, the first row select line and second row select line each running along the length of the row and not being connected to pixels of any other row"**, as disclosed in column 11 lines 18-49 and exhibited in figures 2 and 9-12.

In addition, Hashimoto discloses resetting a voltage level of a node (FD portion) associated with the first pixel (PD1,Mtx1,Mres,Msf,Msel) to a predetermined voltage using a reset transistor (Mres) addressed by a reset line (62) that extends approximately linearly across the pixel array, which reads on claimed, **"resetting a voltage level of a node associated with the first pixel to a predetermined voltage using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array"**, as disclosed in column 10 lines 6-15 and exhibited in figures 9 and 10.

In addition, Hashimoto discloses transferring charge collected by the first pixel (PD1,Mtx1,Mres,Msf,Msel) to the node, which reads on claimed, **"transferring charge collected by the first pixel to the node"**, as disclosed in column 10 lines 16-33 and exhibited in figures 9-12.

In addition, Hashimoto discloses detecting charge at the node, which reads on claimed, **"detecting the charge at the node"**, as disclosed in column 10 lines 16-33 and exhibited in figures 9-12.

In addition, Hashimoto discloses generating an output signal over the shared column line (57) corresponding to the charge detected at the node, which reads on claimed, **"generating an output signal over the shared column line, the output signal corresponding to the image"**, as disclosed in column 11 lines 18-30 and exhibited in figures 9-12.

Regarding claim 85, Hashimoto discloses everything claimed as applied above (see claim 84), in addition, Hashimoto discloses wherein the shared column line (57) extends approximately linearly across the pixel array, which reads on claimed, **"wherein the shared column line extends approximately linearly across the pixel array",** as exhibited in figure 10.

Regarding 86, Hashimoto discloses everything claimed as applied above (see claim 85), in addition, Hashimoto discloses wherein the first and second row select lines (58,59) extend approximately linearly across the pixel array, which reads on claimed, **"wherein the first and second row select lines extend approximately linearly across the pixel array",** as exhibited in figure 10.

Regarding 87, Hashimoto discloses everything claimed as applied above (see claim 84), in addition, Hashimoto discloses wherein the first and second row select lines (58,59) extend approximately linearly across the pixel array, which reads on claimed, **"wherein the first and second row select lines extend approximately linearly across the pixel array",** as exhibited in figure 10.

Regarding claim 88, Hashimoto discloses, **"a plurality of pixels to generate an output signal associated with detected light, the plurality of pixels arranged in rows and columns of an array (fig. 2), each said row having both odd and even pixels, wherein each said odd pixel (PD1,Mtx1,Mres,Msf,Msel) is addressed by a**

respective first address circuit (58,57) consisting essentially of an odd row select line (58) and a shared column line (57), and wherein each said even pixel (PD2,Mtx2,Mres,Msf,Msel) is addressed by a respective second address circuit (59,57) consisting essentially of an even row select line (59) and a shared column line (57), wherein the even row select lines (59) do not address the odd pixels and the odd row select lines (58) do not address the even pixels", as exhibited in figures 2 and 9-12.

In addition, Hashimoto discloses, **"a plurality of column lines (57) comprising the column lines of the first address circuit (58,57) and the second address circuit (59,57), each of the plurality of column lines (57) being connected to at least two adjacent pixels of a row in the array, the column lines (57) being connected to output circuitry (82-87) to output the signal"**, as exhibited in figure 10.

In addition, Hashimoto discloses a column driver (71 and timing controller 25) to address pixels connected to the column lines (57), which reads on claimed, **"a column driver to address pixels connected to the column lines"**, as exhibited in figures 1 and 10.

In addition, Hashimoto discloses a row driver (70) to address pixels through the odd row select lines (58) and the even row select lines (59) , which reads on claimed, **"a row driver to address pixels through the odd row select lines and the even row select lines"**, as exhibited in figure 10.

Regarding claim 89, Hashimoto discloses everything claimed as applied above (see claim 88), in addition, Hashimoto discloses wherein the column lines (57) extend approximately linearly across the array, which reads on claimed, **"wherein the column lines extend approximately linearly across the array",** as exhibited in figure 10.

Regarding claim 90, Hashimoto discloses everything claimed as applied above (see claim 89), in addition, Hashimoto discloses wherein the odd and even row select lines (58,59) extend approximately linearly across the array, which reads on claimed, **"wherein the odd and even row select lines extend approximately linearly across the array",** as exhibited in figure 10.

Regarding claim 91, Hashimoto discloses everything claimed as applied above (see claim 88), in addition, Hashimoto discloses wherein the odd and even row select lines (58,59) extend approximately linearly across the array, which reads on claimed, **"wherein the odd and even row select lines extend approximately linearly across the array",** as exhibited in figure 10.

Regarding claim 92, Hashimoto discloses everything claimed as applied above (see claim 88), in addition, Hashimoto discloses a plurality of reset lines (62) that extend approximately linearly across the array, which reads on claimed, **"a plurality of reset lines that extend approximately linearly across the array",** as exhibited in figures 9 and 10.

Regarding claim 93, Hashimoto discloses, **"providing a first address circuit (59,57) for a even pixels (PD2,Mtx2,Mres,Msf,Msel) of a row of pixels and a second address circuit (58,57) for odd pixels (PD1,Mtx1,Mres,Msf,Msel) of the row of pixels, said first address circuit consisting essentially of an even row select line (59) and a plurality of shared column lines (57), and said second address circuit consisting essentially of an odd row select line (58) and said plurality of shared column lines (57), wherein the even row select lines (59) do not address the odd pixels and the odd row select lines (58) do not address the even pixels"**, as exhibited in figures 9-12.

In addition, Hashimoto discloses addressing even pixels (PD2,Mtx2,Mres,Msf,Msel) in a row of an array of pixels using a row driver (70) coupled to an even row select line (59), which reads on claimed, **"addressing the even pixels using a row driver coupled to the even row select line"**, as exhibited in figure 10.

In addition, Hashimoto discloses providing a first output signal associated with light detected by the even pixels (PD2,Mtx2,Mres,Msf,Msel) to a plurality of column lines (57) coupled to the even pixels (PD2,Mtx2,Mres,Msf,Msel), which reads on claimed, **"providing a first output signal associated with light detected by the even pixels to the plurality of shared column lines"**, as exhibited in figure 10.

In addition, Hashimoto discloses addressing odd pixels (PD1,Mtx1,Mres,Msf,Msel) using the row driver (70) coupled to the odd row select line

(58), which reads on claimed, **"addressing the odd pixels using the row driver coupled to the odd row select line"**, as exhibited in figure 10.

In addition, Hashimoto discloses providing a second output signal associated with light detected by the odd pixels (PD1,Mtx1,Mres,Msf,Msel) to the plurality of column lines (57) coupled to the odd pixels (PD1,Mtx1,Mres,Msf,Msel), which reads on claimed, **"providing a second output signal associated with light detected by the odd pixels to the plurality of shared column lines"**, as exhibited in figure 10.

Regarding claim 94, Hashimoto discloses everything claimed as applied above (see claim 93), in addition, Hashimoto discloses wherein the column lines (57) extend approximately linearly across the array and are approximately orthogonal to both the even row select line (59) and the odd row select line (58), which reads on claimed, **"wherein the column lines extend approximately linearly across the array and are approximately orthogonal to both the even row select line and the odd row select line"**, as exhibited in figure 10.

Regarding claim 95, Hashimoto discloses everything claimed as applied above (see claim 94), in addition, Hashimoto discloses wherein the odd and even row select lines (58,59) extend approximately linearly across the array, which reads on claimed, **"wherein the odd and even row select lines extend approximately linearly across the array"**, as exhibited in figure 10.

Regarding claim 96, Hashimoto discloses everything claimed as applied above (see claim 94), in addition, Hashimoto discloses a plurality of reset lines (62) that extend approximately linearly across the array, which reads on claimed, **"a plurality of reset lines that extend approximately linearly across the array",** as exhibited in figure 10.

Regarding 102, Hashimoto discloses a pixel array comprising a row comprising a plurality of first pixels (PD1,Mtx1,Mres,Msf,Msel) and a plurality of second pixels (PD2,Mtx2,Mres,Msf,Msel), which reads on claimed, **"a pixel array comprising a row of first pixels and second pixels"**, as exhibited in figure 10.

In addition, Hashimoto discloses a respective column line (57) for each pair of first and second pixels of the row; and a reset line (62) connected to the plurality of first pixels, which reads on claimed, **"a first address circuit (58,57) for the first pixels consisting essentially of a first row select line (58) and a plurality of shared column lines (57)"**, as exhibited in figure 10.

In addition, Hashimoto discloses, **"a second address circuit (59,57) for the second pixels consisting essentially of a second row select line (59) and said plurality of shared column lines (57), wherein the first row select lines (58) do not address the second pixels and the second row select lines (59) do not address the first pixels, each of the shared column lines (57) being associated with a first pixel and a second pixel"**, as exhibited in figures 9-12.

In addition, Hashimoto discloses, **"a reset line (62) connected to the first pixels"**, as exhibited in figure 10.

Regarding claim 103, Hashimoto discloses everything claimed as applied above (see claim 102), in addition, Hashimoto discloses wherein the plurality of first pixels are every other pixel in the row, which reads on claimed, **"wherein the plurality of first pixels are every other pixel in the row"**, as exhibited in figures 2 and 10.

Regarding claim 104, Hashimoto discloses everything claimed as applied above (see claim 102), in addition, Hashimoto discloses wherein each pair of first and second pixels of the row are arranged with the first and second pixels positioned adjacent each other along the column line (57), which reads on claimed, **"wherein each pair of first and second pixels of the row are arranged with the first and second pixels positioned adjacent each other along the column line"**, as exhibited in figure 10.

Regarding claim 106, Hashimoto discloses a row of pixels comprising a first plurality of pixels (PD1,Mtx1,Mres,Msf,Msel) and a second plurality of pixels (PD2,Mtx2,Mres,Msf,Msel), a first address line (58) addressing only the first plurality of said pixels and a second address line (59) addressing only the second plurality of said pixels, which reads on claimed, **"a row of pixels comprising a first plurality of pixels and a second plurality of pixels"**, as exhibited in figures 2 and 10.

In addition Hashimoto discloses, **"a first address circuit (58,57) for the first plurality of said pixels and a second address circuit (59,57) for the second plurality of said pixels, said first address circuit consisting essentially of a first**

row select line (58) and a plurality of shared column lines (57), and said second address circuit consisting essentially of a second row select line (59) and said plurality of shared column lines (57), wherein the first row select lines (58) do not address the second plurality of pixels and the second row select lines (59) do not address the first plurality of pixels, each of said plurality of shared column lines (57) being connected to a first pixel of the first plurality of pixels and a second pixel of the second plurality of pixels", as exhibited in figures 2 and 9-12.

In addition, Hashimoto discloses a reset line (62) connected to at least the first plurality of pixels or the second plurality of pixels, which reads on claimed, **"a reset line connected to at least the first plurality of pixels or the second plurality of pixels"**, as exhibited in figures 2 and 10.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 97-101, and 105 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto in view of Brehmer et al. (US Patent 6,130,423) hereinafter referenced as Brehmer further in view of Bird (US Patent 5,721,422) further in view of Shinohara (US Patent 5,587,738).

Regarding claim 97, Hashimoto discloses a row comprising a first pixel (PD1,Mtx1,Mres,Msf,Msel) and a second pixel (PD1,Mtx2,Mres,Msf,Msel); the first and second pixels being joined; a first even row line (59) connected with the first pixel; and a second odd row line (58) connected with the second pixel (58), wherein said first even row line and said second odd row line are associated with said row and not any other row; and a column line (57) connected with the first and second pixels, which reads on claimed, **"a row comprising a first pixel and a second pixel; the first and second pixels being joined...a first even row line connected with the first pixel; a second odd row line connected with the second pixel, wherein said first even row line and said second odd row line are associated with said row and not any other row; and a column line connected with the first and second pixels"**, as exhibited in figures 9 and 10.

However, Hashimoto fails to explicitly disclose that the first and second pixels are joined by a diagonal active area and that the column line is connected at the diagonal active area. However, the examiner maintains that it was well known in the art to provide **"the first and second pixels being joined by a diagonal active area component...a column line connected with the first and second pixels at the diagonal active area"**, as taught by Brehmer and Shinohara.

In a similar field of endeavor Brehmer discloses a method and apparatus for a CMOS image sensor with a distributed amplifier. In addition, Brehmer discloses a pixel

array wherein each pixel includes its own amplifier and has an increased dynamic range, as exhibited in figure 7.

In addition, in a similar field of endeavor Bird discloses electronic devices having an array with shared column conductors. In addition Bird discloses two adjacent pixels sharing a column line between the two pixels to reduce the number of column lines in an image sensor, as disclosed in column 2 lines 1-10 and exhibited in figure 1.

Hashimoto teaches two adjacent pixels sharing an amplifier to prevent decrease in dynamic range and also sharing the same column line. Brehmer teaches pixels each with their own amplifier having a function of increasing dynamic range. Bird teaches two adjacent pixels sharing a column line. Therefore, it would have been obvious to one of ordinary skill in the art to substitute adjacent pixels of Hashimoto having a common amplifier, with the pixels of Brehmer each having their own amplifier, and applying the technique of using a single column line for two adjacent pixels, wherein the column line is provided between the two pixels to achieve the predictable result of a pixel array with increased dynamic range and a reduced number of column lines.

In a similar field of endeavor Shinohara discloses a solid-state image pickup device having plural switches for subtracting a stored signal from a pixel output. In addition, Shinohara discloses a row comprising a first pixel (diffusion layer 44 on the left) and a second pixel (diffusion layer 44 on the right); first and second pixels being joined by a diagonal active area component; a column line (34) connected with the first and second pixels at the diagonal active area component, which reads on claimed, **"the first and second pixels being joined by a diagonal active area component...a**

column line connected with the first and second pixels at the diagonal active area", as disclosed in column 1 lines 42-65 and exhibited in figure 2.

Hashimoto, Brehmer, and Bird, the combination, teaches a pixel array wherein adjacent pixels share a common column line between the two pixels. Shinohara teaches two pixels connected by a diagonal active area wherein a column line is connected to both pixels at the diagonal active area component. Therefore, it would have been obvious to one of ordinary skill in the art to apply the technique of connecting two adjacent pixels with a diagonal active area and connecting a column line at the diagonal active area to the adjacent pixels sharing a column line of the combination to achieve the predictable result of more efficiently resetting all pixels in a selected row line simultaneously and improving performance.

In addition, Hashimoto discloses, **"a first address circuit (59,57) for the first pixel consisting essentially of the first even row select line (59) and a shared column line (57)"**, as exhibited in figure 10.

In addition, Hashimoto discloses, **"a second address circuit (58,57) for the second pixel consisting essentially of the second odd row select line (58) and said shared column line (57), wherein the first even row select line (59) does not address the second pixel and the second odd row select line (58) does not address the first pixel"**, as exhibited in figure 10.

Regarding claim 98, Hashimoto, Brehmer, Bird, and Shinohara, the combination, discloses everything claimed as applied above (see claim 97), in addition, Hashimoto

discloses the row further comprises a plurality of first pixels and a plurality of second pixels, which reads on claimed, **"wherein the row further comprises a plurality of first pixels and a plurality of second pixels",** as exhibited in figure 10.

Regarding claim 99, Hashimoto, Brehmer, Bird, and Shinohara, the combination discloses everything claimed as applied above (see claim 97), in addition, Hashimoto discloses wherein the first even row line (59) and second odd row line (58) each extends substantially linearly across an array of pixels, which reads on claimed, **"wherein the first even row line and second odd row line each extends substantially linearly across an array of pixels",** as exhibited in figure 10.

Regarding claim 100, Hashimoto, Brehmer, Bird, and Shinohara, the combination, discloses everything claimed as applied above (see claim 97), in addition, Hashimoto discloses a first reset line (62) for the first pixel and the second pixel, which reads on claimed, **"a first reset line for the first pixel...and...the second pixel",** as exhibited in figure 10.

However, the combination fails to explicitly disclose two separate reset lines for the first and second pixels. However, the examiner takes official notice of the fact that it was well known in the art at the time of the invention to provide **"a first reset line for the first pixel and a second reset line for the second pixel"**.

Hashimoto teaches a pixel array wherein two adjacent pixels use the same reset line. However, because Hashimoto reads from the first pixel, then resets the floating

diffusion node storing the voltage of the first pixel, then reads from the second pixel, then resets the floating diffusion node storing the voltage of the second pixel, it is in essence performing the equivalent operation of two separate reset lines being executed at separate times. In addition, using separate reset lines for pixels of the same row is well known in the art. Therefore, simply substituting using a single reset line which alternately resets the two pixels, with two separate reset lines which alternately reset the two pixels, would have been obvious to one of ordinary skill in the art and would yield the predictable result of alternately resetting two pixels of the same row.

Regarding claim 101, Hashimoto, Brehmer, Bird, and Shinohara, the combination, discloses everything claimed as applied above (see claim 100), in addition, Hashimoto discloses each of the first even row line (59), second odd row line (58), and first reset line (62) extends substantially linearly across the first and second pixels, which reads on claimed, **"wherein each of the first even row line, second odd row line, first reset line...extends substantially linearly across the first and second pixels",** as exhibited in figure 10.

However, the combination fails to explicitly disclose two separate reset lines for the first and second pixels which both extend linear across the array. However, the examiner takes official notice of the fact that it was well known in the art at the time of the invention to provide **"second reset line extends substantially linearly across the first and second pixels"**.

Hashimoto teaches a pixel array wherein two adjacent pixels use the same reset line. However, because Hashimoto reads from the first pixel, then resets the floating diffusion node storing the voltage of the first pixel, then reads from the second pixel, then resets the floating diffusion node storing the voltage of the second pixel, it is in essence performing the equivalent operation of two separate reset lines being executed at separate times. In addition, using separate reset lines for pixels of the same row which extend linearly across the pixels is well known in the art. Therefore, simply substituting using a single reset line which alternately resets the two pixels, with two separate reset lines which alternately reset the two pixels and extend linearly across the two pixels, would have been obvious to one of ordinary skill in the art and would yield the predictable result of alternately resetting two pixels of the same row.

Regarding 105, Hashimoto discloses a pixel array comprising a row comprising a plurality of first pixels (PD1,Mtx1,Mres,Msf,Msel) and a plurality of second pixels (PD2,Mtx2,Mres,Msf,Msel), which reads on claimed, **"a pixel array comprising a row comprising a plurality of first pixels and a plurality of second pixels"**, as exhibited in figure 10.

In addition, Hashimoto discloses a first row address line (58) connected with the first pixels, which reads on claimed, **"a first row address line connected with the first pixels"**, as exhibited in figure 10.

In addition, Hashimoto discloses a second row address line (59) connected with the second pixels, wherein the second row address line (59) is not connected with the

first pixels and the first row address line (58) is not connected with the second pixels, which reads on claimed, **"a second row address line connected with the second pixels, wherein the second row address line is not connected with the first pixels and the first row address line is not connected with the second pixels"**, as exhibited in figure 10.

In addition, Hashimoto discloses a respective column line (57) for each pair of first and second pixels of the row; and a reset line (62) connected to the plurality of first pixels, which reads on claimed, **"a respective column line for each pair of first and second pixels of the row; and a reset line connected to the plurality of first pixels"**, as exhibited in figure 10.

However, Hashimoto fails to explicitly disclose that the first and second pixels are joined by a diagonal active area. However, the examiner maintains that it was well known in the art to provide **"the first and second pixels are connected by a substantially diagonal active area"**, as taught by Brehmer and Shinohara.

In a similar field of endeavor Brehmer discloses a method and apparatus for a CMOS image sensor with a distributed amplifier. In addition, Brehmer discloses a pixel array wherein each pixel includes its own amplifier and has an increased dynamic range, as exhibited in figure 7.

In addition, in a similar field of endeavor Bird discloses electronic devices having an array with shared column conductors. In addition Bird discloses two adjacent pixels sharing a column line between the two pixels to reduce the number of column lines in an image sensor, as disclosed in column 2 lines 1-10 and exhibited in figure 1.

Hashimoto teaches two adjacent pixels sharing an amplifier to prevent decrease in dynamic range and also sharing the same column line. Brehmer teaches pixels each with their own amplifier having a function of increasing dynamic range. Bird teaches two adjacent pixels sharing a column line. Therefore, it would have been obvious to one of ordinary skill in the art to substitute adjacent pixels of Hashimoto having a common amplifier, with the pixels of Brehmer each having their own amplifier, and applying the technique of using a single column line for two adjacent pixels, wherein the column line is provided between the two pixels to achieve the predictable result of a pixel array with increased dynamic range and a reduced number of column lines.

In a similar field of endeavor Shinohara discloses a solid-state image pickup device having plural switches for subtracting a stored signal from a pixel output. In addition, Shinohara discloses a row comprising a first pixel (diffusion layer 44 on the left) and a second pixel (diffusion layer 44 on the right); first and second pixels being joined by a diagonal active area component; a column line (34) connected with the first and second pixels at the diagonal active area component, which reads on claimed, **"the first and second pixels are connected by a substantially diagonal active area"**, as disclosed in column 1 lines 42-65 and exhibited in figure 2.

Hashimoto, Brehmer, and Bird, the combination, teaches a pixel array wherein adjacent pixels share a common column line between the two pixels. Shinohara teaches two pixels connected by a diagonal active area wherein a column line is connected to both pixels at the diagonal active area component. Therefore, it would have been obvious to one of ordinary skill in the art to apply the technique of connecting

two adjacent pixels with a diagonal active area and connecting a column line at the diagonal active area to the adjacent pixels sharing a column line of the combination to achieve the predictable result of more efficiently resetting all pixels in a selected row line simultaneously and improving performance.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL BERARDESCA whose telephone number is

(571)270-3579. The examiner can normally be reached on Mon- Fri 8:30am-6:00pm EST (Alternate Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571)272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Berardesca
Examiner
Art Unit 2622

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Examiner, Art Unit 2622
May 21, 2009

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